REMARKS

This Amendment responds to the Office Action mailed on July 13, 2006. Claims 1-5, 7-15, and 42-52 are pending. Claims 1, 42, and 47 have been amended. In view of the foregoing amendments, as well as the following remarks, Applicants respectfully submit that this application is in complete condition for allowance and request reconsideration of the application in this regard.

Claim Objection

Applicants have amended claim 1 as suggested by the Examiner. Applicants request that the Examiner withdraw the objection.

Rejections of Claims Under 35 U.S.C. § 102

Appenzeller Rejection

Claims 42-45 stand rejected under 35 U.S.C. §102(e) as anticipated by Appenzeller et al. (U.S. Pub. No. 2005/0056826), hereinafter *Appenzeller*. Claim 42 is the only independent claim. Applicants respectfully traverse this rejection for the reasons set forth below.

Independent claim 42 sets forth "a gate dielectric disposed on said sidewall between said semiconducting nanotube and said gate electrode." The Examiner contends that lines 13-14 of paragraph [0040] in *Appenzeller* disclose a gate dielectric (511) "disposed on the vertical sidewall between the semiconductor nanotube 508 and the right hand side gate electrode 512." In contrast to the Examiner's contention, paragraph [0040] of *Appenzeller* discloses that "a gate dielectric, e.g., 511 can be formed around the nanotubes, e.g., 508, over the metal catalyst 501 and under the sacrificial layer 510." (Emphasis added by Applicants). Paragraph [0040] of *Appenzeller* also discloses that "the gate dielectric can be deposited between the nanotubes" if the nanotubes (508) form a two dimensional array. (Emphasis added by Applicants).

Based upon paragraph [0040] of *Appenzeller*, a person having ordinary skill in the art would recognize that the gate dielectric (511) is disposed around and between the carbon nanotubes (508). *Appenzeller* fails to disclose that the gate dielectric (511) is deposited on the sidewall of the gate electrode (512) , as set forth in Applicants' independent claim 42. Instead, the sidewall of the gate electrode (512) is separated from the nearest portion of the gate dielectric (511) by an unfilled gap or space.

In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. If the reference fails to teach even one of the claimed elements, the reference does not and cannot anticipate the claimed invention. Because *Appenzeller* fails to disclose a structural arrangement in which a gate dielectric is deposited on a sidewall of a gate electrode, *Appenzeller* fails to anticipate independent claim 42. Consequently, Applicants request that the rejection be withdrawn.

Independent claim 42 is patentable for additional reasons. Specifically, the Examiner has failed to appreciate that the gate electrode (512) and spacer (503) that he has identified in *Appenzeller* are three dimensional structures. Specifically, the passage in which the nanotubes (508) are formed is an opening defined in continuous layers (503, 504, 505) of dielectric materials. Referring to paragraph [0039], *Appenzeller* discloses that the nanotubes are grown in a "pore" that "confines" the growth space so that the growth is forced "to follow the vertical direction." The gate electrode (512) is formed by depositing a layer of a conductor, as shown in Fig. 5k of *Appenzeller*, and shaping the deposited conductor layer as shown in Fig. 5l of *Appenzeller*. As a result, the gate electrode (512) has a sidewall that extends about the circumference of the passage in which the nanotubes (508) are disposed. It logically follows that the spacer (503) identified by the Examiner in *Appenzeller* is between the passage in which the nanotubes (508) are disposed and the vertical sidewall of the gate electrode (512). In contrast, Applicants' claim 42 sets forth that the passage in which the nanotubes are disposed is between the vertical sidewall of the gate electrode and the spacer. The Examiner cannot simply ignore the three-dimensional aspects of the structure disclosed in *Appenzeller*.

Because claims 43-45 depend from independent claim 42, Applicants submit these claims are also patentable for at least the same reasons discussed above.

Dubin Rejections

Claims 1, 5, 8, 12-15, 42-45, 47, and 49-52 also stand rejected under 35 U.S.C. § 102(e) as anticipated by Dubin et al. (U.S. Pub. No. 2005/0167755), hereinafter *Dubin*. Claims 1, 42, and 47 are the only independent claims. The Examiner contends that *Dubin* shows or teaches all the elements of the rejected claims. Applicants respectfully disagree for the reasons set forth below.

In contrast to claim 1, *Dubin* does not disclose or suggest a "gate electrode," "a spacer of a dielectric material flanking said vertical sidewall and spaced horizontally from said vertical sidewall of said gate electrode to define a vertical passage," "said semiconducting nanotube positioned in said vertical passage," and "a gate dielectric disposed on said vertical sidewall between said semiconducting nanotube and said gate electrode."

The Examiner contends on page 4 of the Office Action that *Dubin* discloses "a spacer 215 (corresponding to dielectric layer 215 formed on an outer sidewall surface of the ring gate electrode 202) flanking the vertical inner sidewall surface and spaced from the vertical inner sidewall surface of the ring gate electrode 202 to define a vertical passage." The Examiner also contends that "the semiconducting nanotube 250 is positioned in the vertical passage." On page 5 of the Office Action, the Examiner contends that Dubin discloses "a gate dielectric 215 (corresponding to dielectric layer 215 formed on the inner sidewall surface of the ring gate electrode 202) disposed on the vertical inner sidewall surface between the semiconducting nanotube 250 and the gate dielectric 202." The Examiner kindly provides the Applicants with an annotated version of Fig. 5F from *Dubin* on page 5 of the Office Action that indicates the Examiner's identifications of the inner and outer sidewall surfaces of the ring gate electrode (202), the location of the vertical passage, and the spacer formed on the outer sidewall surface of the ring gate electrode (202).

In making these contentions, the Examiner has completely ignored the three-dimensional structure of the elements shown in cross-section in Fig. 5F of *Dubin*. The Examiner has correctly identified the "inner sidewall surface" and the "outer sidewall surface" of the ring-shaped gate electrode (202), as indicated by the Examiner on the annotated version of Fig. 5F from *Dubin* on page 5 of the Office Action. The Examiner has also correctly identified the portion of dielectric layer (215) on the "inner sidewall surface" of the ring-shaped gate electrode (202) as a gate dielectric.

However, the Examiner has not recognized that the gate electrode (202) is shaped like a ring or annulus. As a result, the "inner sidewall surface" of gate electrode (202) identified by the Examiner is a continuous, closed annular surface that encircles the vertical passage in which the carbon nanotube (250a) is located. According to paragraph [0049] of *Dubin*, this "inner sidewall surface" of the ring-shaped gate electrode (202) surrounds a central bore defining a passage in which the carbon nanotube (250a) is disposed. Therefore, in the cross-sectional view of Fig. 5F in *Dubin*, the "inner sidewall surface" is also present between the carbon nanotube (250a) and the spacer (215) identified by the Examiner on the annotated version of Fig. 5F from *Dubin* on page 5 of the Office Action.

The Examiner contends that the spacer (215) is formed on the "outer sidewall surface" of the ring-shaped gate electrode (202). However, the "outer sidewall surface" of the ring-shaped gate electrode (202) is separated from the central bore by the radial width of the ring-shaped gate electrode (202). Hence, the spacer (215) identified by the Examiner actually flanks a different vertical sidewall of the gate electrode (202) than the vertical sidewall of the gate electrode (202) that the Examiner contends includes the gate dielectric.

In contrast, Applicants' claim 1 requires that the sidewall of the gate electrode carrying the gate dielectric is also the same sidewall that the spacer borders to define the passage for the carbon nanotube. In order for a reference to anticipate the invention in a claim, the reference must teach each and every element in the precise arrangement set forth in the claim. If the reference fails to teach even one of the claimed elements, the reference does not and cannot

anticipate the claimed invention. *Dubin* fails to disclose an arrangement in which a gate dielectric is disposed on a sidewall of the gate electrode and that same sidewall is flanked by a spacer to define a passage for a carbon nanotube, as set forth in Applicants' claim 1. For at least this reason, Applicants respectfully request that this rejection be withdrawn.

Because claims 2-5 and 8-15 depend from independent claim 1, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, these claims recite unique combinations of elements not taught, disclosed or suggested by *Dubin*.

Independent claim 42 is patentable for at least the same or similar reasons as independent claim 1. Because claims 43-46 depend from independent claim 42, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, these claims recite unique combinations of elements not disclosed or suggested by *Dubin*.

Independent claim 47 is patentable for at least the same or similar reasons as independent claims 1 and 42. Because claims 49-52 depend from independent claim 47, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, these claims recite unique combinations of elements not disclosed or suggested by *Dubin*.

Rejections of Claims Under 35 U.S.C. § 103

Claims 2-4, 9-11, 46, and 48 stand rejected under 35 U.S.C. § 102(e) as anticipated by or, in the alternative, rejected under 35 U.S.C. § 103(a) as obvious over *Dubin*. Because claims 2-4 and 9-11 depend from independent claim 1, claim 46 depends from independent claim 42, and claim 48 depends from independent claim 47, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, these claims each recite a unique combination of elements not disclosed or suggested by *Dubin*.

Conclusion

Applicants have made a bona fide effort to respond to each and every requirement set forth in the Office Action. In view of the foregoing amendments and remarks, this application is submitted to be in complete condition for allowance and, accordingly, a timely notice of allowance to this effect is earnestly solicited. In the event that any issues remain outstanding, the Examiner is invited to contact the undersigned to expedite issuance of this application.

Applicants do not believe fees are dues in connection with filing this communication. If, however, any fees are necessary as a result of this communication, the Commissioner is hereby authorized to charge any under-payment or fees associated with this communication or credit any over-payment to Deposit Account No. 23-3000.

Respectfully submitted,

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